Expanding KIM-Style 6502 Single Board Computers

Part 1 of 3:
Hal Chamberlin

Undoubtedly the most successful single board computer ever has been the KIM-1 made by MOS Technology (now Commodore). When introduced it apparently had just the right combination of features and price to attract tens of thousands of users. More recently of course the SYM-1 from Synertek and AIM-65 from Rockwell have incorporated numerous additional features into the same self-contained single board computer concept. Fortunately for users, all three of these machines are quite similar in their electrical characteristics.

Sooner or later however all computers need to be expanded and these single board machines are no exception. Although the SYM-1 and AIM-65 can be expanded somewhat merely by plugging in additional memory chips, the maximum limit is only 4K bytes of programmable memory. Thus additional boards are required for substantially increased RAM, ROM, or I/O capability. Recognizing this fact, the computer manufacturers as well as a number of independent accessory manufacturers have designed and brought to market a wide variety of expansion boards for the KIM, SYM, and AIM computers.

In most cases just having expansion boards available is not enough; there must also be a *motherboard* offered to plug them into since these computers have no on-board bus and slot sockets of their own. To date the computer manufacturers and independents have selected no fewer than four distinctly different ways to do this. First on the scene of course was MOS Technology who offered the KIM-4 expansion motherboard which mated with their KIM-2 and KIM-3 expansion memory boards. The bus presented by the KIM-4, which is called the "KIM-4 Bus", is in many ways similar to the bus presented by the computer itself as its own expansion edge connector. The primary difference is an altered pin assignment which is basically a one pin shift from the expansion connector assignments. This apparently was done to provide additional ground connections. Since then, independent manufacturers have also offered KIM-4 style expansion motherboards although there are important differences from the original KIM-4 (see Compute issue #3).

Shortly thereafter, as soon as the KIM's popularity became known, other independent manufacturers offered expansion motherboards which presented an S-100 style bus to the expansion boards. The primary advantage of this approach is that the user is not restricted to using expansion boards designed specifically for KIM-style machines but instead can choose from hundreds of S-100 compatible boards designed for 8080 based systems. Unfortunately many of the more sophisticated S-100 boards such as large dynamic memories, graphic display interfaces, and disk controllers could not be used because of substantial timing differences between 6502 and 8080 style microprocessors.

Late in 1977 Micro Technology Unlimited introduced a motherboard and card cage for the 6502 based single-board computers. The motherboard is little more than 5 edge connectors wired in parallel with one for the computer and the other 4 for expansion boards. The bus presented is the same pinout as that of the processor's expansion connector. The main advantage of this technique is the low cost and compact packaging afforded by the elimination of bus buffers. In addition, expansion boards compatible with this bus may be easily connected directly in parallel with the expansion connector if for some reason the motherboard is not desired. The main disadvantage is that the number of expansion boards is limited to four by the small drive capability of the computer's own bus.

Recently Rockwell has introduced its expansion motherboard which essentially presents an Exorcisor bus to the expansion boards. Motorola originated this bus for use in their Exorcisor microprocessor development systems. Rockwell also uses the Exorcisor bus in their system 65 development system. The advantage of this method, at least to Rockwell, is avoiding the need to develop new expansion boards just for the AIM-65. To users the biggest drawback of the Exorcisor bus probably is the lack of reasonably priced boards to plug into it.

All four of these techniques are quite viable methods for expanding KIM-1, SYM-1, and AIM-65 single board computers and each has a broad base of dedicated users.

Mechanics

All three of the single board computers are intended to simply rest flat on a tabletop using the several quarter-inch high rubber feet provided. Although not the most beautiful thing in the world, it works well in many cases and is certainly inexpensive. In situations where better appearance is desired or small children are present, there are vacuum-forced dress covers available that simply slip over the computer board hiding everything except the display and keyboard.

The KIM-4, S-100, and Exorcisor type expansion motherboards simply extend this board-on-the-table concept. Typically the expansion motherboard is roughly the same size as the computer board and plugs straight onto its expansion connector. On the motherboard are perhaps a dozen integrated circuits for address decoding, bus buffering, and voltage regulation. The majority of the space however is taken up by 4 to 8 edge connectors which form the "slots" of the expansion bus. When plugged into these slots, the expansion boards assume a vertical orientation.

A system expanded this way uses a large amount of additional table space, and in the case of th KIM, it is useful space to the left of the computer. The assembly of interconnected boards is also rather fragile and certainly not portable unless dismantled (most people would probably bolt the computer and motherboard to a sheet of plywood or plastic to avoid this). In particular a stray elbow can do considerable damage if a board is knocked out of its slot during operation. Unfortunately the available plastic dress covers do nothing to protect the added motherboard or expansion boards.

Another approach that has been slowly gaining acceptance is to place the expansion boards underneath and parallel to the computer board. Thus the expansion motherboard, which ties all of the boards together, is vertical. In order to hold this assembly of boards together, an aluminum frame with card guides is typically supplied and the motherboard is attached to an opening in the frame. Figures 1 and 2 show the KIM and AIM versions respectively of Micro Technology's implementation of this concept.

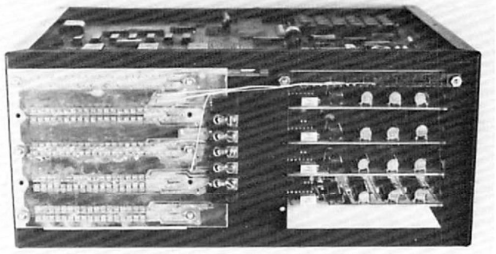

FIG. 1 KIM-1 INSTALLED IN A MICRO TECHNOLOGY UNLIMITED MOTHERBOARD/CARD FILE

The advantages of this configuration of course are reduced table space requirements and greatly increased protection for the expansion boards. The entire assembly of computer and boards is now one portable unit with only the power supply left over to worry about. The computer board is still exposed however. Probably the only potential disadvantage is that the computer's keyboard has been raised about 4 inches above the tabletop.

Electronics

There are electronic factors to consider as well when expanding a KIM, SYM, or AIM computer. In order to minimize cost, complexity, and power consumption, all three of these single board computers are designed without buffers between the microprocessor chip and the expansion edge connector. The KIM-1 went one step further and omitted part of the address decoding circuitry as well. The lack of buffers means that the expansion bus presented by these computers has a DC drive capability of only one standard TTL load, or equivalently, 5 low power Shottky loads. The AC drive capability depends on the desired signal rise-time. For bus operation at 1mHz, a total of approximately 25 "connections" at 6pF each can be driven. A connection here is defined as a gate input, disabled tri-state output, or MOS input (which does not contribute to DC loading).

Compared to other bus-oriented computers, such as S-100 machines, this does not sound like much of a bus at all since these machines typically have a drive capability of 30 standard TTL loads (74 series) or nearly 150 low power Shottky (74LS series) or over 200 low power TTL (74L series) loads. In fact, the original advertising for the MITS Altair computer boasted an expansion capacity of "over 200 boards". While this may have seemed necessary when using MITS's 1K memory and single port I/O boards, 10 slots is ample for even the largest S-100 setup when using today's dense memory and peripheral interface boards.

Over the years, experience has shown that several factors other than sheer driver power limit the number of boards that may be connected to a bus.

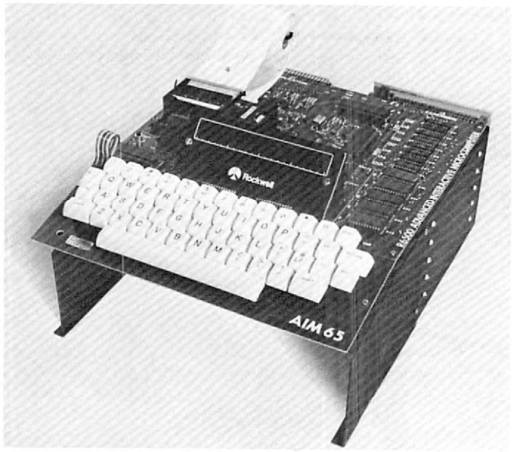

FIG. 2. AIM-65 INSTALLED IN A MICRO TECHNOLOGY UNLIMITED MOTHERBOARD/CARD FILE

The most serious of these is crosstalk noise between the bus address/data lines and the various bus con-

trol lines. This noise arises when large numbers of address and data lines change state simultaneously, which is a common occurrence. The fast voltage risetimes (around 5NS with the popular 8T97 drivers) and 50MA or greater surges of current along each changing line couple electrostatically and magnetically to other lines in the bus and on the expansion boards themselves. Longer busses and more boards plugged in gradually increase the crosstalk until noise on the control lines causes false triggering of memory and I/O boards and thus system failure. So severe is this problem that early S-100 systems would fail to operate even before the 16 board capacity of a single cabinet was reached.

A related, but much less severe problem, is signal reflection from the ends of the bus lines, which after all, act like transmission lines. This effect becomes significant when the signal transmission time exceeds about 1/2 of the signal risetime. At 1.5NS per foot with a 5NS risetime, the bus would have to be two feet long before termination was required. The apparent success of bus terminators sold for S-100 systems is probably due to their reduction of signal swings (the logic 1 level is limited to 3 volts and floating bus lines are pulled to 3 volts) which in turn reduces crosstalk noise.

From the author's experience in designing a large, fast bus oriented system (specifically the A. B. Dick Magna SL four terminal full-page word processing computer), there are three ways to solve bus noise problems. One is to thoroughly shield the bus with a full-width ground plane, or ideally, a three-layer motherboard with data/address on one side, ground in the middle, and control signals on the other side. This solves noise coupling on the bus but not on the expansion boards which in turn must be carefully designed to minimize their own crosstalk. This technique was used in the Magna SL machine because of speed requirements.

Another technique is to use filters and delays on the control signals obtained from the bus in order to reject narrow noise pulses. This technique can be extended to deal with any kind of noise problem at the expense of system speed and is the one typically used with minicomputers such as DEC PDP-11's and Data General NOVA's.

The third technique attacks the source of the noise, namely fast risetimes and large current surges, by using a low power bus. With liesurely risetimes of 50 to 100NS and drive capabilities of less than 10MA, such a bus is virtually noise-free and quite fast enough for normal microprocessor operation. This technique, coupled with some attention to groundplane shielding, is most applicable to unbuffered KIM/SYM/AIM expansion busses.

The foregoing is not meant to imply that all of the buffered expansion motherboards available for the KIM, SYM, and AIM computers are racked with noise. In fact, their bus length and number of slots is generally small enough to keep noise at tolerable levels. The major point is that high power drivers and indefinitely expandable busses do have drawbacks of their own.

The real question at this point then is: How many expansion boards can the unbuffered microprocessor bus drive before becoming overloaded? The 6502 microprocessor is rated to drive slightly more than 1 standard TTL load (equivalent to five low power shottky loads) on its address and data busses while most of the RAM's and ROM's tied to the data bus can drive two standard TTL loads. The 6520, 6522, and 6530 I/O chips have the same drive capability as the microprocessor. Thus in general the answer is at least four boards provided that the expansion boards themselves buffer the bus such that only one low power shottky load (.36MA in the zero state) is presented to the bus by the board. Many boards on the market and particularly those designed for an unbuffered bus do this. Actually, any well designed board would be expected to buffer the bus in order to provide clean signals for the remainder of the board logic. The reason that only four boards can be driven instead of five is that some of the address lines are loaded by a low power Shottky decoder IC on the computer board itself. ©

Next time: The Great Experiment

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Editor's Note: Hal ended his first installment with this · · ·

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The Great Experiment

Of course loading the microprocessor with a full five loads puts the system right at the limit of rated drive current. One of the problems with testing digital circuitry is that there is no obvious indication of marginal operation that may later develop into a full fledged failure as components age. In order to determine the actual drive limit, the author took a fully stuffed AIM-65 (4K on-board RAM, assembler ROM and BASIC ROM's) and started adding Micro Technology K-1016 16K memory boards, the idea being to add boards until failure due to bus overload occurred. These boards use low power Shottky buffers onboard so each one would be expected to add a .36MA load to the bus.

Since the AIM's 40K of free addresses would only accomodate two of these boards, the most significant address bit was cut away from the bus at each socket position and instead connected to parallel output bits on the AIM's application connector. The boards were then jumpered to respond to addresses between 2000 and 5FFFF (hex). By programming only one output bit to be low at a time, a rudimentary bank switching setup was implemented. When the system was reset, all output bits automatically go high thus disabling all of the boards and preventing interference with the AIM monitor (since A15 was ignored, an enabled board would also respond to A000-DFFFF). A proper bank switch setup would have required a two-input OR gate (negative AND) to be tied to each of the A15 pins. In any case, it was adequate to run a memory test program.

The first trial was to install 4 of the 16K boards which worked fine as expected. Next, another card file was placed below the first and jumper wires added between the two motherboards. This gave a total of 9 bus slots which were filled with 16K memory boards. Again the memory test program (which wrote all 144K of memory with random data before reading any of it back) indicated no problem and the AIM monitor and BASIC continued to work flawlessly. A check with an oscilloscope revealed minimal signal degradation.

Finally, a third card file was added and bus jumpers installed to give a total of 14 slots. Three additional 16K memory boards were scrounged (I had no idea that more than 9 or 10 boards could be driven) to give a total of 192K of RAM. Again there were no obvious problems and the bus was being loaded to three times rated capacity! Figure 3 shows what the stack of card files looked like which is obviously impractical unless one cuts a hole in the tabletop to let the two extra card files hang below (I simply sat on a drafting stool to use the system). The rear view in figure 4 shows the interconnected motherboards and individual Board Enables from the application connector. Note the gridwork of copper braid between motherboards which makes the groundplane essentially continuous between the motherboards.

Photographs of the address and data bus signals were taken while running the memory test program and are shown in figure 5. About the only visible loading effect on the address bus is a long tail on the zero-to-one transition during phase 1 of the clock. The data bus appears to be even cleaner with just a shade over 100NS required for the data to stabilize after the leading edge of phase 2. The microprocessor was driving the data bus for the data bus for this photo (scope synced to read/write line on the bus). The zero logic levels, which one would think show the effect of gross overloading most, were still in the 0.3 volt range although the one levels were down to only 3 volts from a normal lightly loaded value of nearly 4 volts. Note the almost complete absence of noise. These "overloaded" signals actually look far better than most S-100 bus signals!

While these results are encouraging and certainly show that a four board load does not bring a system to the brink of failure, it does not mean that loading rules can be disregarded altogether. Some AIM's, as well as SYM's and KIM's, can be expected to have a weak component on-board that may not be able to drive a 12 board load adequately for reliable operation. Thus the "official" recommendation is to stick with the spec book and limit unbuffered systems to four boards. However, individual hobbyists should be able to go one or two boards over the limit with little probability of problems. Actually, addressing limitations are more likely to limit system size than bus drive capability with today's dense boards.

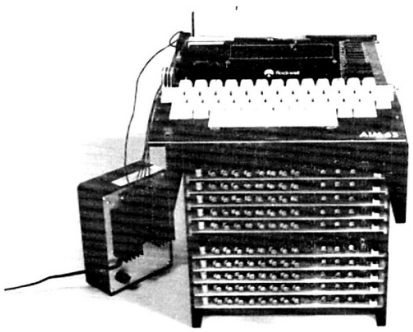


FIG.3.FRONT VIEW OF 192K RAM TEST SYSTEM

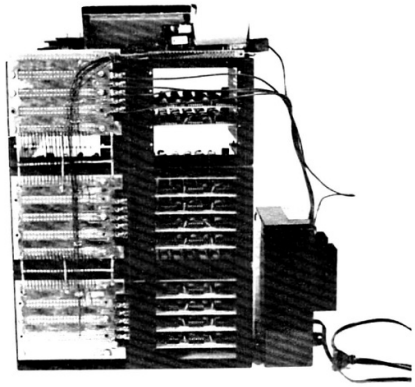
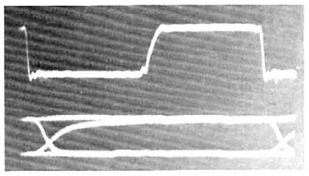
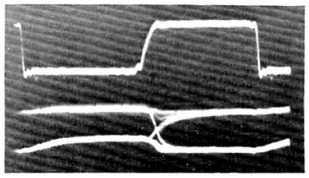


FIG. 4. REAR VIEW OF 192K TEST SYSTEM SHOWING MOTHERBOARDS WIRED TOGETHER



A.
ADDRESS
BUS



B.
DATA
BUS

FIG. 5. BUS SIGNAL WAVEFORMS IN 192K TEST SYSTEM. TOP WAVEFORM IN EACH PHOTO IS PHASE 2 CLOCK.

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The Modified KIM Bus

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This leads us to a definition of the "Unbuffered Modified KIM Bus". KIM is part of the name since the bus is essentially what a KIM-1 single board computer presents on its expansion connector. "Modified" is part of the name because not all of the 44 signals on the expansion connector are actually part of the bus. Those signals that are part of the bus are common to the SYM and AIM computers as well as the KIM and thus any of these machines may be plugged into the bus without modification.

Figure 6 gives a signal listing for the bus. Signals marked with an * do not connect to the processor but do connect to all of the other boards in the system. Most of these have different specialized functions on the different processors anyway and are not generally useful in a bus oriented system. Note that RDY is one of the signals that is not bussed. All modern memories are quite fast enough to operate without wait states in 6502 systems and besides, the 6502 will not wait during write cycles anyway. The lines marked (Reserved) are intended for future uses such as memory bank switching signals, etc.

Note that although RAM R/W is listed as a signal (should go low during phase 2 of Write cycles), it should not be used by a bus interface board for general application. The reason is that an AIM-65 printed circuit error makes it go low during *read* cycles rather than write cycles like it should. In any case, one should be able to design any kind of bus interface board using just A0 - A15, D0 - D7, R/W, PHASE 2, interrupt, and power voltages. The additional lines are really just convenience signals.

Two of the signals are important only in KIM systems. DECODE ENABLE must go low whenever addresses between 0000 and 1FFF are on the bus in order to activate KIM's on-board memory. VECTOR FETCH must go low whenever addresses between FFFA and FFFF are on the bus in order for the reset/interrupt vectors stored in the KIM monitor ROM's to be active. Although it is probably best for the motherboard to generate these two signals, many expansion boards generate them anyway so that the bus motherboard can be omitted altogether in systems with just one expansion board.

Note that direct memory access is not supported by the Modified KIM Bus because the address lines from the 6502 cannot be disabled. An approach to DMA in those interfaces that need it, such as video displays and disk controllers, is to provide *two-port memory* on the interface board itself. The big advantage then is that DMA to or from the on-board memory can then proceed at very high speed without slowing the processor at all. A conventional DMA system, such as on S-100 systems, would stop the processor cold at data rates beyond a couple of hundred thousand bytes per second.

Although +5 volts regulated is available on the bus, it is often preferable to use unregulated +8 and an on-board regulator to provide +5 to the logic circuitry of expansion boards. Similarly, +16 unregulated is available for generating +12 power needed by many memory chips. When negative voltages are needed such as for EPROM's or analog circuitry, they may be easily generated from the positive unregulated voltages with a charge-pump circuit and then regulated with IC regulators. The primary advantages of on-board regulation are a smaller and less expensive central power supply and clean, well regulated power on the expansion board itself. The potential problem of additional heat dissipation on the expansion boards is nullified by the very low power consumption of modern LS IC's.

PIN	KIM-1	SYM-1	AIM-65	MODIFIED
E-1	SYNC	SYNC	SYNC	SYNC
E-2	RDY	RDY	RDY	(reserved)
E-3	PHASE 1	PHASE 1	PHASE 1	(reserved)
E-4	IRQ	IRQ	IRQ	IRQ
E-5	SET OVERFLOW	SET OVERFLOW	SET OVERFLOW	SET OVERFLOW
E-6	NMI	NMI	NMI	NMI
E-7	RESET	RESET	RESET	RESET
E-8	DATA BUS 7	DATA BUS 7	DATA BUS 7	DATA BUS 7
E-9	DATA BUS 6	DATA BUS 6	DATA BUS 6	DATA BUS 6
E-10	DATA BUS 5	DATA BUS 5	DATA BUS 5	DATA BUS 5
E-11	DATA BUS 4	DATA BUS 4	DATA BUS 4	DATA BUS 4
E-12	DATA BUS 3	DATA BUS 3	DATA BUS 3	DATA BUS 3
E-13	DATA BUS 2	DATA BUS 2	DATA BUS 2	DATA BUS 2
E-14	DATA BUS 1	DATA BUS 1	DATA BUS 1	DATA BUS 1
E-15	DATA BUS 0	DATA BUS 0	DATA BUS 0	DATA BUS 0
E-16	K6	30	+12 VOLTS REG.	* (reserved)
E-17	SINGLE STEP OUT	DB CUT	+12 VOLTS REG.	* (reserved)
E-18	(N.C.)	POWER ON RESET	CS5	* +7.5 UNREG
E-19	(N.C.)	(N.C.)	CS5	* VECTOR FETCH
E-20	(N.C.)	(N.C.)	CSA	* DECODE ENABLE
E-21	+5 VOLT REG.	+5 VOLT REG.	+5 VOLT REG.	+5 VOLT REG.
E-22	GROUND	GROUND	GROUND	GROUND
E-A	ADDR BUS 0	ADDR BUS 0	ADDR BUS 0	ADDR BUS 0
E-B	ADDR BUS 1	ADDR BUS 1	ADDR BUS 1	ADDR BUS 1
E-C	ADDR BUS 2	ADDR BUS 2	ADDR BUS 2	ADDR BUS 2
E-D	ADDR BUS 3	ADDR BUS 3	ADDR BUS 3	ADDR BUS 3
E-E	ADDR BUS 4	ADDR BUS 4	ADDR BUS 4	ADDR BUS 4
E-F	ADDR BUS 5	ADDR BUS 5	ADDR BUS 5	ADDR BUS 5
E-H	ADDR BUS 6	ADDR BUS 6	ADDR BUS 6	ADDR BUS 6
E-J	ADDR BUS 7	ADDR BUS 7	ADDR BUS 7	ADDR BUS 7
E-K	ADDR BUS 8	ADDR BUS 8	ADDR BUS 8	ADDR BUS 8
E-L	ADDR BUS 9	ADDR BUS 9	ADDR BUS 9	ADDR BUS 9
E-M	ADDR BUS 10	ADDR BUS 10	ADDR BUS 10	ADDR BUS 10
E-N	ADDR BUS 11	ADDR BUS 11	ADDR BUS 11	ADDR BUS 11
E-P	ADDR BUS 12	ADDR BUS 12	ADDR BUS 12	ADDR BUS 12
E-R	ADDR BUS 13	ADDR BUS 13	ADDR BUS 13	ADDR BUS 13
E-S	ADDR BUS 14	ADDR BUS 14	ADDR BUS 14	ADDR BUS 14
E-T	ADDR BUS 15	ADDR BUS 15	ADDR BUS 15	ADDR BUS 15
E-U	PHASE 2	PHASE 2	PHASE 2	PHASE 2
E-V	READ/WRITE	READ/WRITE	READ/WRITE	READ/WRITE
E-W	READ/WRITE	READ/WRITE	READ/WRITE	READ/WRITE
E-X	PLL TEST	AUDIO TEST	AUDIO TEST	* +16 VOLT UNREG.
E-Y	PHASE 2	PHASE 2	PHASE 2	PHASE 2
E-Z	RAM R/W	RAM R/W	# RAM R/W	RAM R/W

* These signals are not bussed to the CPU slot.
\# Signal generated is different from KIM-1 and SYM-1.

Fig. 6 Processor and Modified Expansion Bus Signals